Enhanced Pulse Width Modulation

1. ePWM Module Overview

TMS320F28379D Microcontroller

What is ePWM?

Enhanced Pulse Width Modulation

Hardware-based PWM generation

Configurable frequency and duty cycle

Advanced control and protection features

ePWM in the F28379D

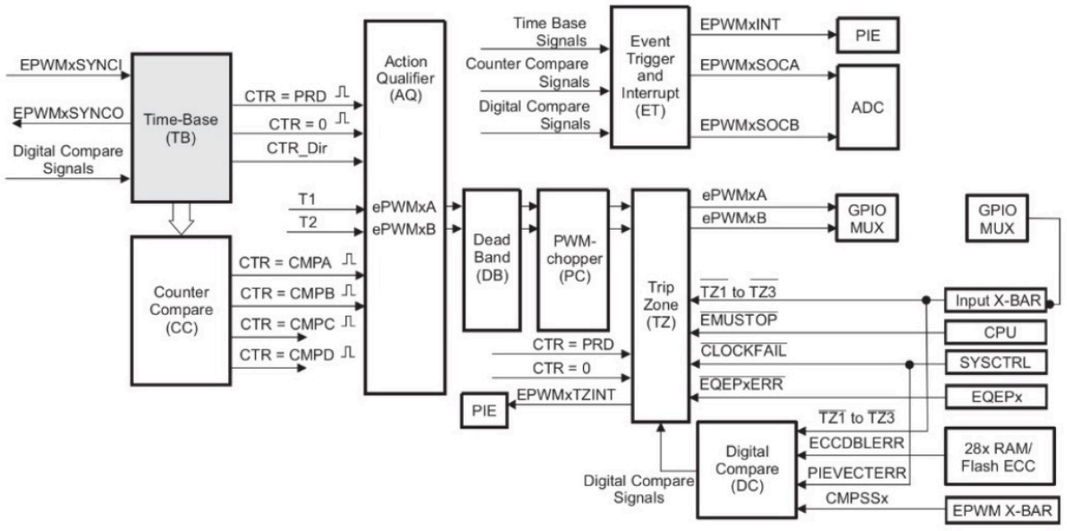
12 independent ePWM modules

ePWM1 to ePWM12

Controlled by CPU1 or CPU2

Multiple configurable submodules

ePWM Architecture



Time-Base (TB)

Counter-Compare (CC)

Action Qualifier (AQ)

Dead-Band (DB)

Event Trigger (ET)

Trip-Zone (TZ)

Advanced ePWM Features

Event Trigger (ET)

Interrupts and ADC triggers

Dead-Band (DB)

Complementary switching delays

Trip-Zone (TZ)

Fault detection and protection

Summary

- The Time Base Sub-module generates the carrier waveform and also sets the PWM frequency.
- The Event Trigger and Interrupt Sub-module generates interrupts and can also start converting measured analog signals to digital form.
- The Counter Compare Sub-module performs a fine comparison between the carrier waveform and four possible values that can be modulation signals or duty ratios.
- The Action Qualifier Sub-module can be used to decide what action (gating signals) to take based on comparison results.
- The Dead Band Sub-module can be used to insert a dead band between complementary gating signals to prevent a shoot-through fault.
- The Trip Zone Sub-module can turn off the gating signals based on fault feedback or user off signals.

2. Preparing the ePWM Module

- Before configuring the ePWM module, a few preparations need to be made.
- There is a maximum limit to the clock frequency that the ePWM module can accept as input. This differs from the processor's maximum clock (200 MHz).
- Since the ePWM module is shared, we must decide which CPU controls it. By default, it is CPU1.
- Once we decide which CPU controls the ePWM module, we must enable the clock signal to the ePWM module in the peripheral clock control register of that CPU.

ePWM Clock Frequency

		MIN	NOM	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		200[(2)]	MHz
$t_{c(SYSCLK)}$	Period, device (system) clock	5[(2)]		500	ns
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	120		400	MHz
$f_{(AUXPLLRAWCLK)}$	Frequency, auxiliary PLL output (before AUXCLK divider)	120		400	MHz
$f_{(AUXPLL)}$	Frequency, AUXPLLCLK	2	60	60	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		200[(2)]	MHz
$f_{(LSP)}$	Frequency, LSPCLK	2		200[(2)]	MHz
$t_{c(LSPCLK)}$	Period, LSPCLK	5[(2)]		500	ns
$f_{(OSCCLK)}$	Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1)		See respective clock		MHz
$f_{(EPWM)}$	Frequency, EPWMCLK[(1)]			100	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		100	MHz

The maximum ePWM clock frequency is 100 MHz.
The maximum processor clock frequency is 200 MHz.

ePWM Clock Divider
PERCLKDIVSEL Register

Figure 3-156. PERCLKDIVSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	EMIF2CLKDIV	RESERVED	EMIF1CLKDIV	RESERVED		EPWMCLKDIV	
R-0-0h	R/W-1h	R-0-0h	R/W-1h	R/W-0h		R/W-1h	

EPWMCLKDIV determines the ePWM clock divider.
EPWMCLKDIV = 0 → EPWMCLK = SYSCLK
EPWMCLKDIV = 1 → EPWMCLK = SYSCLK / 2
For SYSCLK = 200 MHz, use EPWMCLKDIV = 1.

ePWM CPU Selection

CPUSEL0 Register

Figure 3-126. CPUSEL0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	EPWM12	EPWM11	EPWM10	EPWM9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EPWM8	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

The ePWM modules can be controlled by CPU1 or CPU2.
By default, all ePWM modules are assigned to CPU1.
Bit = 0 → CPU1
Bit = 1 → CPU2

ePWM Peripheral Clock

PCLKCR2 Register

Figure 3-167. PCLKCR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	EPWM12	EPWM11	EPWM10	EPWM9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EPWM8	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Each ePWM module has an individual clock enable bit.
The controlling CPU must enable the corresponding peripheral clock.
Bit = 0 → Clock disabled
Bit = 1 → Clock enabled

ePWM Clock Synchronization

PCLKCR0 Register

Figure 3-165. PCLKCR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED				GTBCLKSYNC	TBCLKSYNC	RESERVED	HRPWM
R-0-0h				R/W-0h	R/W-0h	R-0-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		CPUTIMER2	CPUTIMER1	CPUTIMER0	DMA	RESERVED	CLA1
R-0-0h		R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

TBCLKSYNC → Time-Base clock synchronization
GTBCLKSYNC → Global Time-Base clock synchronization
TBCLKSYNC = 1 → Start the ePWM Time-Base clocks.
GTBCLKSYNC = 1 → Start ePWM Time-Base clocks globally in synchronization.
GTBCLKSYNC overrides TBCLKSYNC.

3. Time Base Sub-module

The Time Base Sub-module sets up the carrier waveform through a counter similar to the timers in the previous section.

The timers in the Time Base Sub-module can count in different directions: up (sawtooth), down (reverse sawtooth), and up-down (triangular).

The Time Base Sub-module can synchronize with either an external pin or other ePWM modules.

The Time Base Sub-module cannot generate interrupts like the timers in the previous section.

The simplest example will use the Time Base Sub-module in combination with the Counter Compare Sub-module and the Action Qualifier Sub-module.

Time Base Sub-module

TBPRD Register

Figure 15-128. TBPRD Register

15	14	13	12	11	10	9	8
TBPRD							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBPRD							
R/W-0h							

16-bit period register.
This period register is mirrored by default.
This means another register acts as a clone.
Any reads or writes to TBPRD are actually from or to the mirror register.
The mirror register's value is loaded into TBPRD at a scheduled time, so writing to TBPRD does not change the switching-cycle interval mid-cycle.

Time Base Sub-module
TBCTL Register

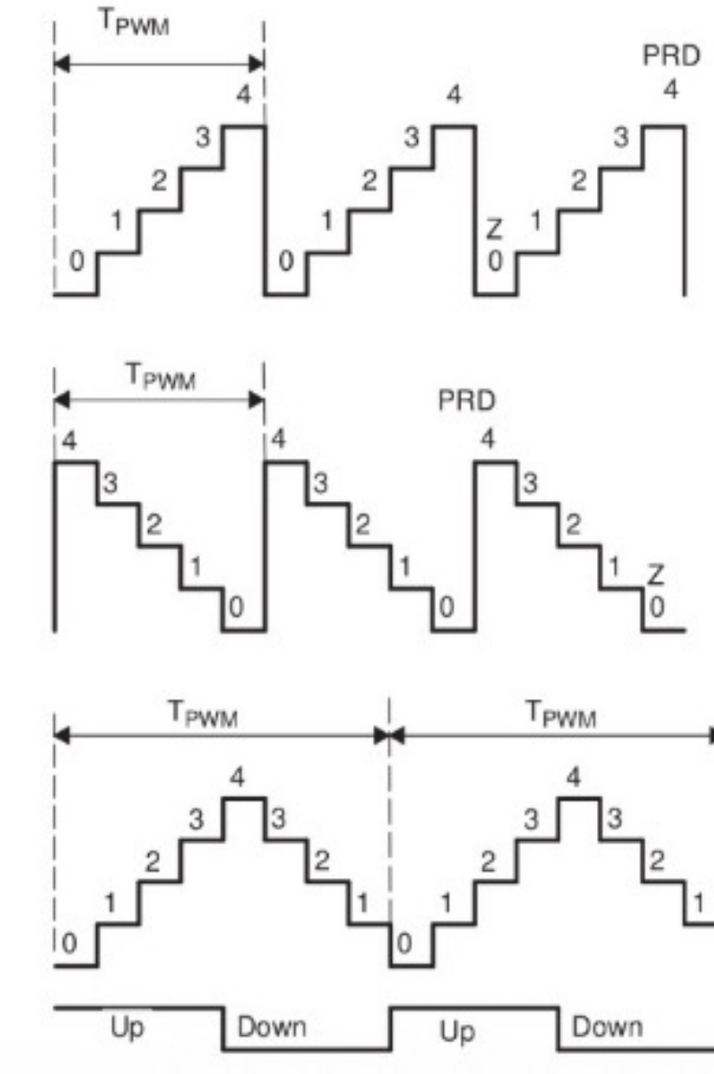
Figure 15-94. TBCTL Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR	CLKDIV			HSPCLKDIV	
R/W-0h		R/W-0h	R/W-0h			R/W-1h	

7	6	5	4	3	2	1	0
PCLKDIV	SWFSYNC	SYNCOSEL		PRDLD	PHSEN	CTRMODE	
R/W-1h	R-0/W1S-0h	R/W-0h		R/W-0h	R/W-0h	R/W-3h	

Bits 14–15 (FREE_SOFT) are similar to the timer. FREE = 1 implies a free-running timer.
Bits 10–12 (CLKDIV) provide the option of dividing EPWMCLK when generating slower switching-frequency gating signals.
Bits 7–9 (HSPCLKDIV) also provide the option of dividing EPWMCLK when generating slower switching-frequency gating signals.
Bit 2 (PHSEN), bits 4–5 (SYNCOSEL), bit 6 (SWFSYNC), and bit 13 (PHSDIR) are related to the synchronization feature.

Time Base Sub-module
Counter Modes — CTRMODE



Bits 0–1 (CTRMODE) determine how the counter will count.

CTRMODE = 0 (00): The counter counts upwards from 0 to the value in the period register, then returns to 0 and starts again.

CTRMODE = 1 (01): The counter counts downwards from the value in the period register to 0, then returns to the period value and starts again.

CTRMODE = 2 (10): The counter counts upwards from 0 to the value in the period register, then counts down to 0 and starts again.

CTRMODE = 3 (11): The counter is stopped (default).

Time Base Sub-module

Period Load — PRDLD

Bit 3 (PRDLD) is the Period Load Bit.

This determines when to load the period mirror register value into the period register TBPRD.

By default, when we write to the PRD register, we write to the mirror register PRDM. This is shadow mode.

This feature prevents disturbances if a write to the period register occurs during a PWM cycle.

The change is reflected only when the counter becomes 0. This occurs at the end of a cycle (down mode) or at the beginning of a cycle (up and up-down modes).

Setting PRDLD to 1 enables immediate load mode, where any write to the period register takes effect immediately, even in the middle of a cycle.

Time Base Sub-module

TBSTS Register

Figure 15-97. TBSTS Register

14	13	12	11	10	9
RESERVED					
R-0-0h					

6	5	4	3	2	1	
RESERVED				CTRMAX	SYNCI	
R-0-0h				R/W1C-0h	R/W1C-0h	

The TBSTS register indicates the timer's status.
CTRDIR is a read-only bit. It is 0 if the counter is counting down and 1 if it is counting up.
The processor sets CTRMAX when the counter reaches the maximum value: 0xFFFF.